R.V.R & J.C.COLLEGE OF ENGINEERING (Autonomous)

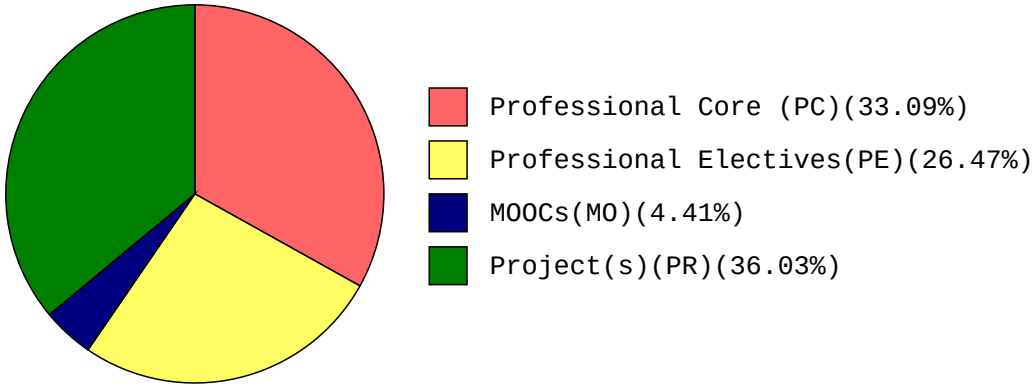
DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

MTECH - VLSI

(w.e.f. the batch of students admitted from the academic year 2025-2026)

Programme Curriculum (R-25) grouping based on course components

Course Component	Curriculum Content (% of total number of credits in programme)	Total number of contact hours	Total number of credits
Professional Core (PC)	33.09	27	22.5
Professional Elective(s) (PE)	26.47	18	18
Project(s) (PR)	36.03	3	24.5
MOOC's (MO)	4.41		3
Mandatory Course(s) (MC)	--	2	--
Total number of Credits			68



R.V.R & J.C.COLLEGE OF ENGINEERING (Autonomous)

MTECH - VLSI

Course Structure, Scheme of Instruction (R25) and Examination

(w.e.f. the batch of students admitted from the academic year 2025-2026)

I Year I Semester **COURSE STRUCTURE**

SNo.	Course Details		Scheme of Instruction			Scheme of Examination			Category Code
	Code No.	Subject Name	Periods per week			Maximum Marks		Credits	
			L	T	P	CIA	SEE		
1	VL511	CMOS Digital IC Design	3	-	-	40	60	3.0	PC
2	VL512	Device Modelling	3	-	-	40	60	3.0	PC
3	VL513	Digital System Design	3	-	-	40	60	3.0	PC
4	VL514	Professional Elective-I	3	-	-	40	60	3.0	PE
5	VL515	Professional Elective-II	3	-	-	40	60	3.0	PE
6	VL516	Professional Elective-III	3	-	-	40	60	3.0	PE
7	VL551	Digital System Design Lab	-	-	3	40	60	1.5	PC
8	VL552	Analog VLSI Design-1 Lab	-	-	3	40	60	1.5	PC
		TOTAL	18	0	6	320	480	21	TPW-24

I Year II Semester **COURSE STRUCTURE**

SNo.	Course Details		Scheme of Instruction			Scheme of Examination			Category Code
	Code No.	Subject Name	Periods per week			Maximum Marks		Credits	
			L	T	P	CIA	SEE		
1	VL521	Analog VLSI Design	3	-	-	40	60	3.0	PC
2	VL522	ASIC Design	3	-	-	40	60	3.0	PC
3	VL523	Physical Design Automation	3	-	-	40	60	3.0	PC
4	VL524	Professional Elective-IV	3	-	-	40	60	3.0	PE
5	VL525	Professional Elective-V	3	-	-	40	60	3.0	PE
6	VL526	Professional Elective-VI	3	-	-	40	60	3.0	PE
7	VL561	Analog VLSI Design-2 Lab	-	-	3	40	60	1.5	PC
8	VL562	Mini Project	-	-	3	40	60	1.5	PR
9	MC	Research Methodology and IPR	2	-	-	100	-	0.0	MC
		TOTAL	18	0	6	320	480	21	TPW-24
Internship 4-8 weeks (Mandatory) during summer vacation (to be evaluated during next semester)									

II Year I Semester **COURSE STRUCTURE**

SNo.	Course Details		Scheme of Instruction			Scheme of Examination		Credits	Category Code
	Code No.	Subject Name	Periods per week			Maximum Marks			
			L	T	P	CIA	SEE		
1	VL611	MOOCs	-	-	-	-	100	3.0	MO
2	VL651	Internship	-	-	-	40	60	3.0	PR
3	VL652	Dissertation Phase-I	-	-	-	40	60	6.0	PR
		TOTAL	0	0	0	80	220	12	TPW-0

II Year II Semester **COURSE STRUCTURE**

SNo.	Course Details		Scheme of Instruction			Scheme of Examination		Credits	Category Code
	Code No.	Subject Name	Periods per week			Maximum Marks			
			L	T	P	CIA	SEE		
1	VL661	Dissertation Phase-II	-	-	-	40	60	14.0	PR
		TOTAL	0	0	0	40	60	14	TPW-0

CIA - Continuous Internal Assessment; SEE - Semester End Examinations

TPW - Total periods per Week

Professional Elective Courses

Code No.	Subject Name	Code No.	Subject Name
VLEL01	Advances in VLSI Design	VLEL02	VLSI Testing
VLEL03	System Verilog	VLEL04	Static Timing Analysis
VLEL05	Low Power VLSI Design	VLEL06	System-on-Chip Design
VLEL07	Scripting Languages for VLSI Design Automation	VLEL08	Machine Learning in VLSI Cad
VLEL09	High Speed VLSI Design	VLEL10	Cpld and Fpga Architectures
VLEL11	CMOS RF Circuit Design	VLEL12	VLSI Design for Signal Processing