(12) PATENT APPLICATION PUBLICATION
(19) INDIA
(22) Date of filing of Application :25/01/2023

(21) Application No.202341005141 A
(43) Publication Date : 03/02/2023

(54) Title of the invention : DESIGN OF HIGH THROUGHPUT AND LOW LATENCY DOUBLE PRECISION FLOATING POINT ARITHMETIC UNIT FOR SPACE SIGNAL APPLICATIONS

(51) International classification :G06F0009300000, G06F0009380000, G06F0007483000, G06F0007499000, G06F0030331000
(86) International Application No :PCT// Filing Date :01/01/1900
(87) International Publication No : NA
(61) Patent of Addition to Application Number :NA Filing Date :NA
(62) Divisional to Application Number :NA Filing Date :NA

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(57) Abstract :
Abstract For space signal processing systems, reliability, accuracy, and performance are major concerns for the detection of accurate phase estimation, for and most of the functionality of the system, the data is acquiring high speed and supervising continuously for validation of correct data. For more accuracy, fixed points arithmetic operations have got lot of data losses and single-precision floating point operations also has data losses. All existing double- precision floating point arithmetic operations utilizes dual rail coding to perform complete detections and required the circuit to receive acknowledge on completion execution and it leads to worst-case delay irrespective of the actual completion time. With help of modified double precision floating point operations, we can obtain more reliability by using memory-based synchronization architecture and high accurate phase detection. In space applications, milli degree estimation is major challenge and plays important role, to estimation milli degree, the Double Precision Floating Point (DPFP) based arithmetic operations are designed using Verilog hardware description language and synthesized with help of Xilinx Design Suite 14.7 ISE software tool and finally implemented on Virtex- FPGA development board. All arithmetic operations use ternary logic at lower-level module design to optimize area and latency. The proposed architecture of double precision floating point arithmetic operations is good enough in terms of power optimization, high speed, optimal delays, hardware utilizations (Slices and LUT's) and smaller-sized edge device. The synthesized results show that proposed DPFP based ALU design for estimation of milli-degree reduces the overall latency to 23%, throughput is improved by 13% and power consumption is reducing to 31% as compared to existing works.

No. of Pages : 11 No. of Claims : 8