(12) PATENT APPLICATION PUBLICATION
(19) INDIA
(22) Date of filing of Application :11/08/2021

(21) Application No.202111036217 A
(43) Publication Date : 03/09/2021

(54) Title of the invention : A SYSTEM HAVING SYNCHRONOUS SIGNALING FOR INTERFACING VLSI CIRCUITS

(51) International classification	:G11C0007100000, G11C0007220000, G06F0013376000, G11C0011407600, G11C0008000000
(31) Priority Document No	:NA
(32) Priority Date	:NA
(33) Name of priority country	:NA
(86) International Application No Filing Date	:NA :NA
(87) International Publication No	: NA
(61) Patent of Addition to Application Number Filing Date	:NA :NA
(62) Divisional to Application Number Filing Date	:NA :NA

(71)**Name of Applicant :**
1)Dr.Rupali Singh
Address of Applicant :Assistant Professor, Department of Electronics and Communication Engineering, SRM Institute of Science & Technology, Delhi-NCR Campus, Modinagar, Ghaziabad, Uttar Pradesh, India. Pin Code:201204 Uttar Pradesh India
2)Dr.Suresh Kumar Pittala
3)Dr.P.Muthu
4)Dr.S.Latha
5)Dr.K.B.S.D Sarma
6)Mr.Tanikonda Kishore Kumar
7)Dr.Sushma Jaiswal
8)Mr.Tarun Jaiswal
9)Mr.Syed Javeed Basha
10)Mr.N.Naveen Sagar
(72)**Name of Inventor :**
1)Dr.Rupali Singh
2)Dr.Suresh Kumar Pittala
3)Dr.P.Muthu
4)Dr.S.Latha
5)Dr.K.B.S.D Sarma
6)Mr.Tanikonda Kishore Kumar
7)Dr.Sushma Jaiswal
8)Mr.Tarun Jaiswal
9)Mr.Syed Javeed Basha
10)Mr.N.Naveen Sagar

(57) Abstract :
The present invention discloses a system having synchronous signaling for interfacing VLSI circuits. The system includes, but not limited to, a synchronous memory device connected to a clock receiver circuitry to receive external clock signals from an external bus for a VLSI circuit; a clock producing circuitry communicatively coupled to the clock receiver circuitry, for producing an internal clock signal having a clock edge which is synchronized with the external clock signal and generates another internal clock signal having a clock edge which is synchronized with the other external clock signal and providing a VLSI interface. Further, the synchronous memory device is having a plurality of sense amplifiers for data latching from a one memory cell location to the other memory cell location in response to a read request from the VLSI interface.

No. of Pages : 22 No. of Claims : 9